



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,748	02/16/2000	Raj Kumar Singh	RAL9-99-0181	6579
25299	7590	07/16/2003		
IBM CORPORATION PO BOX 12195 DEPT 9CCA, BLDG 002 RESEARCH TRIANGLE PARK, NC 27709			EXAMINER THANGAVELU, KANDASAMY	
			ART UNIT 2123	PAPER NUMBER
			DATE MAILED: 07/16/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/505,748	SINGH ET AL.
	Examiner	Art Unit
	Kandasamy Thangavelu	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 April 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-12 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 16 February 2000 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

1. This communication is in response to the Applicants' Response mailed on April 17, 2003. Claims 1, 2, 7, 8 and 9 were amended. Claims 1-12 of the application are pending.

Response to Arguments

2. Applicant's arguments filed on April 17, 2003. have been fully considered. Applicants' arguments, filed on April 17, 2003 under 35 U.S.C. §103 (a) are persuasive. The art rejections are based on the additional prior art included in this office action. Therefore, this office action is made non-final.

Drawings

3. The drawings filed on February 16, 2000 are acceptable subject to correction of the informalities indicated on the "Notice of Draftperson's Patent Drawing Review," PTO-948, sent on December 18, 2002 with paper No. 4.

Specification

4. The disclosure is objected to because of the following informalities:
At Page 2 Lines 17-18, "testing with multiple vendors' of framers" appears to be incorrect and appears that it should be "testing with framers from multiple vendors".

At Page 6 Line 19-20, "testing with multiple vendors' of framers" appears to be incorrect and appears that it should be "testing with framers from multiple vendors".

At Page 10, Line 18, "Many vendors' framer provide" appears to be incorrect and appears that it should be "Many vendors' framers provide".

Appropriate corrections are required.

Claim Objections

5. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

Claims 1-12 are objected to because of the following informalities:

Claim 1, Line 9, "which provide testing with said framers" appears to be incorrect and appears that it should be "which provide for testing with said framers".

In Claim 4, Line 2, "due to constrains stemming from the protection" appears to be incorrect and appears that it should be "due to constraints stemming from the protection".

In Claim 5, Lines 2-4, "customized behavior model, and said model offering" appears to be incorrect and appears that it should be "customized behavior model, said model offering".

In Claim 7, Line 9, "which provide testing with said framers" appears to be incorrect and appears that it should be "which provide for testing with said framers".

In Claim 10, Line 2, "due to constraint stemming from the protection" appears to be incorrect and appears that it should be "due to constraints stemming from the protection".

In Claim 11, Lines 2-4, "further includes the steps of:
develop an accurate customized behavior model,
and
said model offering" appears to be incorrect and appears that it should be "further includes the step of:
developing an accurate customized behavior model,
said model offering".

Claims objected to but not specifically addressed are objected to based on their dependency to an objected claim.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

Art Unit: 2123

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 4, 5, 7 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Seawright et al. (SE)** (U.S. Parent 5,920,711) in view of **Kim et al (KI)** (IEEE, August 1999).

8.1 **SE** teaches System for Frame-based protocol, graphical capture, synthesis, analysis and simulation. Specifically, as per claim 1, **SE** teaches a computer based system employing a customizable simulation model of an ATM/SONET framer, for system level verification and performance characterization (Abstract Lines 1-7); comprising:

means for developing an accurate customizable model that offer sufficient parameters which can be programmed to represent framers from different vendors (Abstract Lines 4-10; Col 3, Lines 16-20).

SE does not expressly teach means for providing two independently configurable components, a Receiver and a Transmitter which provide testing with the Framers from multiple vendors, by changing programmable parameters of the model. **KI** teaches means for providing two independently configurable components, a Receiver and a Transmitter which provide testing

with the Framers from multiple vendors, by changing programmable parameters of the model (Page 25, Col 2, Para 2 and Para 3; Fig. 1; Fig.5 and 6), as all communications between the ATM and the SONET have a transmit path and a receive path (Fig. 1; Fig 5; Page 27, Col 2, Para 6 and 7). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** with the computer based system of **KI** that included means for providing two independently configurable components, a Receiver and a Transmitter which provide testing with the Framers from multiple vendors, by changing programmable parameters of the model, as all communications between the ATM and the SONET have a transmit path and a receive path.

8.2 As per Claim 4, **SE** and **KI** teach the system of Claim 1. **SE** teaches that the system solves problems of observability and controllability, due to constraints stemming from the protection of proprietary data (Abstract Lines 1-7).

8.3 As per Claim 5, **SE** and **KI** teach the system of Claim 4. **SE** teaches that the solution to the problems of observability and controllability, is to develop an accurate customized behavioral model, the model offering sufficient parameters which can be programmed to represent framers of different vendors (Abstract Lines 1-10).

8.4 As per claim 7, **SE** teaches a computer based method employing a customizable simulation model of an ATM/SONET framer, for system level verification and performance characterization (Abstract Lines 1-7) ; comprising the steps of:

developing an accurate customizable model that offers sufficient parameters which can be programmed to represent framers from different vendors (Abstract Lines 4-10; Col 3, Lines 16-20).

SE does not expressly teach providing two independently configurable components, a Receiver and a Transmitter, which provide testing with the Framers from multiple vendors, by changing programmable parameters of the model. **KI** teaches providing two independently configurable components, a Receiver and a Transmitter which provide testing with the Framers from multiple vendors, by changing programmable parameters of the model (Page 25, Col 2, Para 2 and Para 3; Fig. 1; Fig.5 and 6), as all communications between the ATM and the SONET have a transmit path and a receive path (Fig. 1; Fig 5; Page 27, Col 2, Para 6 and 7). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **SE** with the method of **KI** that included providing two independently configurable components, a Receiver and a Transmitter which provide testing with the Framers from multiple vendors, by changing programmable parameters of the model, as all communications between the ATM and the SONET have a transmit path and a receive path.

8.5 As per claims 10 and 11, these are rejected based on the same reasoning as claims 4 and 5, supra. Claims 10 and 11 are computer based method claims reciting the same limitations as claims 4 and 5, as taught throughout by **SE** and **KI**.

9. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Seawright et al. (SE)** (U.S. Parent 5,920,711) in view of **Kim et al (KI)** (IEEE, August 1999),

and further in view of **Bagheri et al. (BA)** (IEEE, May 1995).

9.1 As per Claim 2, **SE** and **KI** teach the system of Claim 1. **KI** teaches that the ATM/SONET Framer provides at least one Receiver and at least one Transmit interfaces to the network at a SONET line rate of 155.52 Mbps(OC-3), 622.08 Mbps(OC-12) (Page 25, Col 1, Para 3; Fig.1; Page 25, Col 2, Para 2 and 3).

SE and **KI** do not expressly teach that the ATM/SONET Framer provides at least one Receiver and at least one Transmit interfaces to the network at a SONET line rate of 2488.32 Mbps(OC-48). **BA** teaches that the ATM/SONET Framer provides at least one Receiver and at least one Transmit interfaces to the network at a SONET line rate of 2488.32 Mbps (OC-48) (Page 427, Col 1, Para 2), as SONET multiplexers are capable of multiplexing information at 2488.32 Mbps due to recent advances in high speed electronics and light wave systems (Page 427, Col 1, Para 2). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** and **KI** with the computer based system of **BA** that included the ATM/SONET Framer provides at least one Receiver and at least one Transmit interfaces to the network at a SONET line rate of 2488.32 Mbps (OC-48), as SONET multiplexers are capable of multiplexing information at 2488.32 Mbps due to recent advances in high speed electronics and light wave systems.

9.2 As per claim 8, it is rejected based on the same reasoning as claim 2, supra. Claim 8 is computer based method claim reciting the same limitations as claim 2, as taught throughout by **SE**, **KI** and **BA**.

10. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Seawright et al. (SE)** (U.S. Parent 5,920,711) in view of **Kim et al (KI)** (IEEE, August 1999), and further in view of **Koziotis et al. (KO)** (IEEE, October 1999),

10.1 As per Claim 3, **SE** and **KI** teach the system of Claim 1. **SE** and **KI** do not expressly teach that the ATM and the SONET interfaces operate on different clock frequencies and represent two distinct clock domains, and the data interchange between the two the clock domains is achieved by means of FIFO buffer elements and associated control and status signals. **KO** teaches that the ATM and the SONET interfaces operate on different clock frequencies and represent two distinct clock domains, and the data interchange between the two the clock domains is achieved by means of FIFO buffer elements and associated control and status signals (Page 1833,Col 1, Para 2; Col 2, Para 3; Fig 1; Page 1834,Col 1, Table 1), as that allows burst read and write independently of external speed and the FIFO provide for speed adaptation and minimize the latency (**KI**: Page 25,Col 2, Para4 to Page 26, Col 1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** and **KI** with the computer based system of **KO** that included the ATM and the SONET interfaces operating on different clock frequencies and representing two distinct clock domains, and the data interchange between the two the clock domains being achieved by means of FIFO buffer elements and associated control and status signals, as that would allow burst read and write independently of external speed and the FIFO would provide for speed adaptation and minimize the latency.

10.2 As per claim 9, it is rejected based on the same reasoning as claim 3, supra. Claim 9 is computer based method claim reciting the same limitations as claim 3, as taught throughout by **SE, KI and KO**.

11. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Seawright et al. (SE)** (U.S. Parent 5,920,711) in view of **Kim et al (KI)** (IEEE, August 1999), and further in view of **Zwan et al. (ZW)** (U.S. Patent 5,991,270), **Bagheri et al. (BA)** (IEEE, May 1995), **Koziotis et al. (KO)** (IEEE, October 1999), **Vogel (VO)** (U.S. Patent 6,075,788), and **Platt (PL)** (U.S. Patent 5,802,073).

11.1 As per Claim 6, **SE** and **KI** teach the system of Claim 4. **KI** teaches the system offers programmability features of delays associated with clock domain synchronization (Page 25, Col 2, Para 4 page 26, Col 1, Para 1).

SE does not expressly teach the computer based system offers programmability and rich feature set and two independently configurable models, one each for the transmit side and the receive side. **KI** teaches the computer based system offers programmability and rich feature set (Page 26, Col 1, Para 3). **KI** teaches the computer based system offers two independently configurable models, one each for the transmit side and the receive side (Page 25, Col 2, Para 2 and Para 3; Fig. 1; Fig.5 and 6), as all communications between the ATM and the SONET have a transmit path and a receive path (Fig. 1; Fig 5; Page 27, Col 2, Para 6 and 7). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the

computer based system of **SE** with the computer based system of **KI** that offered two independently configurable models, one each for the transmit side and the receive side, as all communications between the ATM and the SONET have a transmit path and a receive path.

SE and **KI** do not expressly teach that the computer based system offers programmability features of SONET line rates (OC-Nc: N=1 48; OC-1=51.48 Mbps). **ZW** teaches that the computer based system offers programmability features of SONET line rates (OC-Nc: N=1 48; OC-1=51.48 Mbps) (Col 1, Lines 35-41 and Col 6, Lines 30-40), as it is desirable to produce a test device that can fully test and evaluate each of these formats within a single platform (Col 1, Lines 35-41). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** and **KI** with the computer based system of **ZW** that offered programmability features of SONET line rates (OC-Nc: N=1 48; OC-1=51.48 Mbps), as it would be desirable to produce a test device that can fully test and evaluate each of these formats within a single platform.

SE and **KI** do not expressly teach that the computer based system offers programmability features of percentage of data bytes vs. overhead bytes per row. **BA** teaches that the computer based system offers programmability features of percentage of data bytes vs. overhead bytes per row (Page 427, Col 2, Para 2; Fig. 1), as the frame format varies for various STS levels ((Page 427, Col 2, Para 2). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** and **KI** with the computer based system of **BA** that offered programmability features of percentage of data bytes vs. overhead bytes per row, the frame format varies for various STS levels.

Art Unit: 2123

SE and **KI** do not expressly teach that the computer based system offers programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update. **KO** teaches that the computer based system offers programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update (Page 1833, Col 1, Para 2; Col 2, Para 1 Page 1834, Col 1, Table 1), as that allows burst read and write independently of external speed and the FIFO provide for speed adaptation and minimize the latency (**KI**: Page 25, Col 2, Para 4 to Page 26, Col 1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** and **KI** with the computer based system of **KO** that offered programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update, as that would allow burst read and write independently of external speed and the FIFO would provide for speed adaptation and minimize the latency.

SE and **KI** do not expressly teach that the computer based system offers programmability features of UTOPIA Level-2/3. **VO** teaches that the computer based system offers programmability features of UTOPIA Level-2/3 (Col 5, Lines 59-64), as ATM Forum specifies those standards (Col 5, Lines 59-64). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** and **KI** with the computer based system of **KO** that offered programmability features of UTOPIA Level-2/3, as ATM Forum specifies those standards.

Art Unit: 2123

SE and **KI** do not expressly teach that the computer based system offers programmability features of built-in performance checking. **PL** teaches that the computer based system offers programmability features of built-in performance checking (Abstract; Fig. 1A; Col 1, Line 65 to Col 2, Line 1), as built-in test logic can be used to achieve a high percentage of fault coverage for the whole chip (Col 1, Lines 57-59). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **SE** and **KI** with the computer based system of **PL** that offered programmability features of built-in performance checking, as built-in test logic can be used to achieve a high percentage of fault coverage for the whole chip.

11.2 As per claim 12, it is rejected based on the same reasoning as claim 6, supra. Claim 12 is computer based method claim reciting the same limitations as claim 6, as taught throughout by **SE**, **KI**, **ZW**, **BA**, **KO**, **VO** and **PL**.

Applicant's Arguments

12. The applicant argues the following:

- (1) Rostoker does not teach means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent Framers from different vendors;
- (2) Koziortis does not teach means for providing two independently configurable components, a Receiver and a Transmitter which provide testing with said Framers from multiple vendors, by changing programmable parameters of said model;

(3) Kim does not teach means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent Framers from different vendors; and

(4) the Examiner's combination is improper in that there is no suggestion or motivation in any of the references as to how to combine the teachings from each of the references; the Examiner has not set forth any concrete or logical reasons why an artisan would form the combination.

Examiner's reply

13. As per the applicant's arguments, the applicant's attention is requested to the corresponding claim rejections. In addition, the following explanation is provided to further explain the examiner's position.

13.1 The applicant's argument that "Rostoker does not teach means for developing an accurate customizable behavioral model that offer sufficient", is found persuasive. The examiner has used a new reference (SE).

13.2 The applicant's argument that "Koziortis does not teach means for providing two independently configurable components, a Receiver and a Transmitter which provide testing with said Framers from multiple vendors, by changing programmable parameters of said model", is found persuasive. The examiner has used KI as the reference, which provides both a receiver and a transmitter in the ATM/SONET interfaces that are simulated using Verilog models.

13.3 The applicant's argument that "Kim does not teach means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent Framers from different vendors", is found persuasive. The examiner has used a new reference (**SE**).

13.4 The applicant's argument that "the Examiner's combination is improper in that there is no suggestion or motivation in any of the references as to how to combine the teachings from each of the references; the Examiner has not set forth any concrete or logical reasons why an artisan would form the combination", is found persuasive. The applicants' attention is requested to the relevant motivations provided in the rejections based on combinations.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents and papers are cited to further show the state of the art with respect ATM/SONET (SDH) framers, their design variations and their simulation.

1. Killian et al., "Automated processor generation system for designing a configurable processor and method for the same", U.S. Patent 6,477,683.
2. Shaw et al., "Information processing system for directing information request ...", U.S. Patent 6,349,297.

3. Parson et al., "Simulation model using object oriented programming", U.S. Patent 6,053,947.

4. Calderon et al., "Implementation of a SDH STM-N IC for B-ISDN using VHDL based synthesis tools", ACM, September 1994.

5. Genoe et al., "On the use of VHDL-based behavioral synthesis for telecom ASIC design", ACM, September 1995.

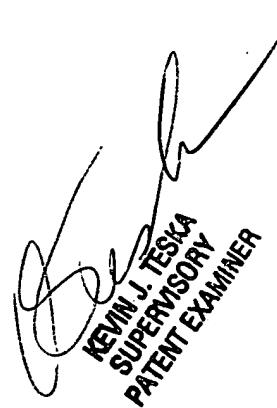
6. Silburt et al., "Accelerating concurrent hardware design with behavioral modeling and system simulation", ACM, January 1995.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-73210.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
June 28, 2003



KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER